

INTEGRATED CIRCUIT TESTING WITH A VISUAL INDICATOR

Abstract of the Disclosure

5 Wafer level testing is accomplished by using a visual indicator (43)
in lieu of a probe machine. Before singulation, each die (52) in a wafer
(50) is placed into a test mode and BIST circuitry (39) in each die
performs predetermined tests of the other circuits on the die. A pass/fail
signal is communicated to a visual indicating device, such as an LED, on
10 the wafer. Each die has a corresponding visual indicator. The LED may
be contained either on the die or in the scribe area. Multiple LEDs may
be used for multiple circuit modules under test. The test permits easy
detection of failures without using probing. Testing such as burn-in may
be performed to determine whether a part will survive a range of
15 operating conditions. In one form, a CMOS implementation of an LED
may be used in conjunction with a CMOS wafer.